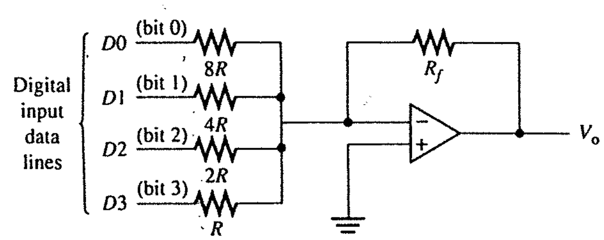
Figure Problem 6.33



Digital inputs = 5 volts for binary 1
= 0 volts for binary 2

$$V_o = -\frac{R_f}{R}\left[D3 + \tfrac{1}{2}D2 + \tfrac{1}{4}D1 + \tfrac{1}{8}D0\right]$$

$$V_{LSB} = -\frac{R_f}{R}\left[\tfrac{1}{8}D0\right]$$

$$V_{MSB} = -\frac{R_f}{R}[D3]$$

$$V_{FS} = 2V_{MSB}$$

Digital input	V_o	Digital input	V_o
0000	0	1000	FS/2
0001	FS/16	1001	9FS/16
0010	FS/8	1010	5FS/8
0011	3FS/16	1011	11FS/16
0100	FS/4	1100	3FS/4
0101	5FS/16	1101	13FS/16
0110	3FS/8	1110	7FS/8
0111	7FS/16	1111	15FS/16

◆ **Figure 6.32** A 4-bit binary-weighted D/A converter. Weighting is provided by input resistors *R*, 2*R*, 4*R*, and 8*R*. Each digital input (*D*0–*D*3) has a value of 0 or 5 V, depending on the corresponding bit in the input code. The output is the weighted sum of only those inputs that have a value of 5 V.

$$V_{MSB} = \frac{-R_f V_1}{R} \tag{6.50}$$

$$V_{FS} = 2 \times V_{MSB} \tag{6.51}$$

$$V_{LSB} = \frac{V_{MSB}}{2^n} \tag{6.52}$$

Although simple to understand, there are many disadvantages to the binary-weighted DAC. Each input resistor has a different resistance based upon the ratio of *R*–2*R*–4*R*–8*R*, and so on. It is difficult to build IC resistors that can be accurately matched at ratios greater than 20:1. This limits binary-weighted DACs to 5 bits or less. Precision resistors or 10-turn potentiometers could be used, but that would be expensive. In addition, each binary bit position is represented by a different Thévenin equivalent resistance, and the devices that provide the inputs to the DAC will see different loads.